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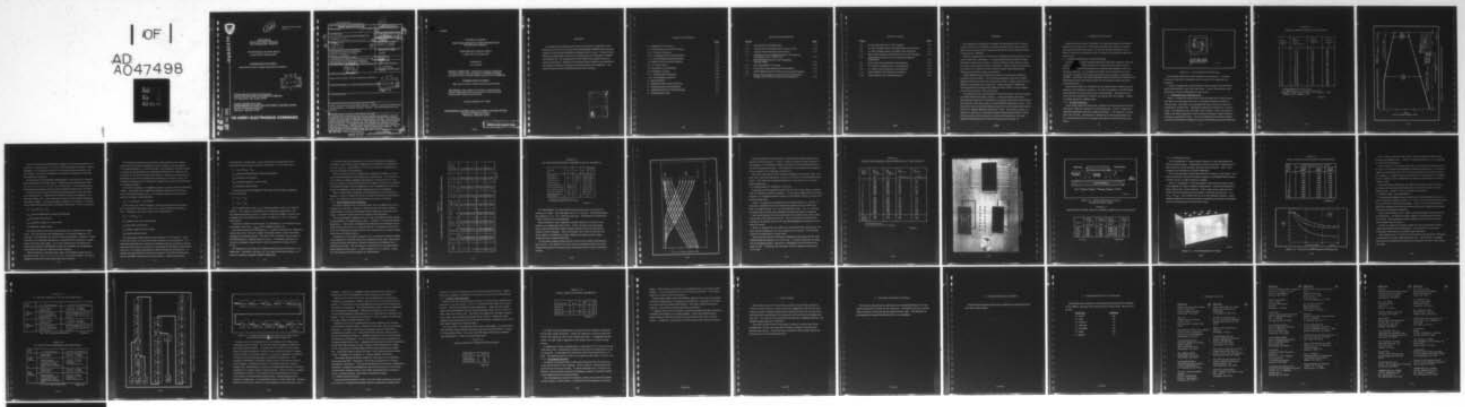

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Fourth Quarterly Progress Report
1 April 1977 to 30 June 1977

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TECHNICAL REPORT

MNOS BORAM MANUFACTURING METHODS AND TECHNOLOGY PROJECT

Fourth Quarterly Progress Report

1 April 1977 to 30 June 1977

Prepared by

J.E. Brewer

PROJECT OBJECTIVE: Establish a production capability for metal nitride oxide semiconductor (MNOS) integrated circuits for block oriented random access memory (BORAM).

Contract DAAB07-76-C-0048

WESTINGHOUSE DEFENSE AND ELECTRONIC SYSTEMS CENTER
Systems Development Division
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ABSTRACT

A manufacturing methods project has been initiated to establish a pilot production line for metal nitride oxide semiconductor (MNOS) block oriented random access memory (BORAM) multichip hybrid circuits. During the past quarter the integrated circuit die for engineering and confirmatory samples were fabricated. All component parts for engineering samples were procured or fabricated. Hybrid circuit thermal characteristics were examined, and memory transistor performance characteristics were explored. The chip and hybrid circuit manufacturing flow were finalized.

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PURPOSE

The purpose of manufacturing methods and technology (MM&T) project number 2769758 is to establish a production capability for metal nitride-oxide semiconductor (MNOS) integrated circuits for block-oriented random access memory (BORAM).

Military organizations are faced with a difficult hardware problem in the use of modern day computers. A suitable militarized secondary storage technology simply does not exist. Drums and discs cannot stand up under the stress of the ground mobile environment. Military real time programs are forced to be resident in main memory because electromechanical storage access delays cannot be tolerated.

MNOS BORAM holds considerable promise of meeting the military's secondary storage needs. An advanced development Army/Navy MNOS BORAM module has proven that significant volume, weight, power and use flexibility advantages can be achieved. When compared to fixed-head electromechanical storage MNOS BORAM offers MTBF's 10 times longer, and access times about 500 times faster.

This MM&T project will establish for the government a source of supply for MNOS BORAM secondary storage. A pilot production line with a demonstrated capacity of 1,875 hybrid circuit per month will be established. Each hybrid circuit will contain 16 MNOS BORAM integrated circuits. This production rate will provide sufficient hybrid circuits to allow fabrication of three 16.8 megabit BORAM modules per month. The hybrid circuits will conform to Electronics Command Technical Requirement SCS503, and the MM&T project will be conducted in accord with Electronics Command Industrial Preparedness Procurement Requirement Number 15.

1. NARRATIVE AND DATA

Progress has been made in production of required samples and detailed definition of the pilot line. This report presents some details of the performance of the MNOS structure, reviews the thermal properties of the hybrid, comments on revisions to the VT tester, and outlines the pilot production line.

1.1 CHARACTERISTICS OF LPCVD DEVICES

The uniform thickness and characteristics achievable using low pressure chemical [illegible]or deposition (LPCVD) for nitride processing led to use of LPCV[illegible]nufacture the second set of engineering samples and the confirmatory samples. To investigate the major device properties actually achieved, a sample of 20 devices was taken from two wafers in production lot 0801. In this case the nitride deposition was performed by a subcontractor. Measurements were performed on the test structures of these previously unscreened 20 die.

Each BORAM 6002 die incorporates a test pattern which contains several capacitor and transistor structures. For this investigation, two 6002 chips were mounted in a single dual-in-line 16-pin package. One memory transistor and one nonmemory transistor on each die was wire bonded. Figure 1-1 shows the pin out configuration.

1.1.1 Nitride Uniformity

As an initial characterization step, capacitor structures on each die were measured to obtain an estimate of nitride thickness. Table 1-1 shows the measured capacitance and the computed thickness. The capacitor area was 100 x 150 microns. The dielectric constant of nitride was assumed to be 6.5, and the permittivity of free space was taken as 8.854E-12 farads per meter.

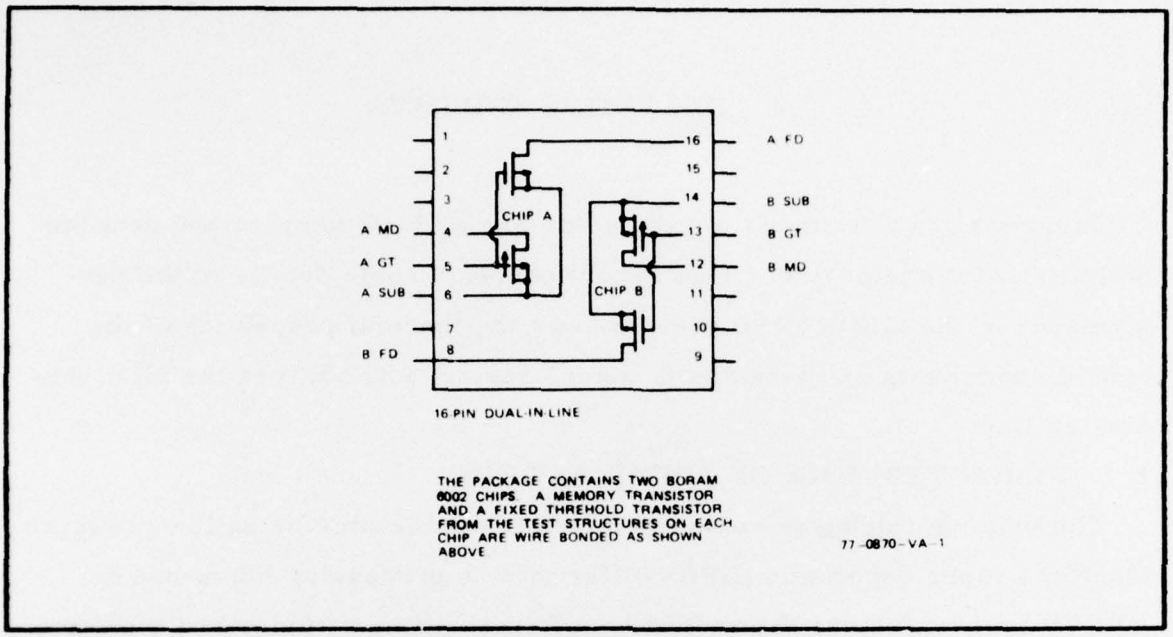

Figure 1-1. Test Sample Pin Identification

The thickness uniformity of the samples was quite good. A standard deviation of less than 5 angstroms about a mean of 511 angstroms was computed.

A series of exploratory measurements of pulse response and threshold decay characteristics were then undertaken. Various computations were performed to aid in interpretation of the results.

1.1.2 Threshold Decay Characteristics

Figure 1-2 shows the typical form of the threshold decay characteristic. The upper curve presents the decay of the high conduction threshold or cleared state. The lower curve presents the decay of the low conduction threshold or written state. Threshold voltages are measured at 10 microamps. The abscissa is the read delay time in hours. Hours are used instead of the device physicist's usual practice of seconds, because BORAM retention is specified in hours. The test conditions and the data presentation format were chosen to approximate practical BORAM application conditions.

TABLE 1-1

NITRIDE THICKNESS FOR LOT 0801 SAMPLE

Device Reference Number	Sample Identification Number (wafer-package-chip)	Nitride Capacitor Measurement C pF	Nitride Thickness Calculation X_n Å
1	2–1A	16.8	514
2	2–1B	17.0	508
3	2–2A	16.6	520
4	2–2B	17.05	506
5	2–3A	16.5	523
6	2–3B	16.9	511
7	2–4A	16.8	514
8	2–4B	17.1	505
9	2–5A	17.0	508
10	2–5B	16.7	517
11	10–1A	16.8	514
12	10–1B	17.0	508
13	10–2A	17.1	505
14	10–2B	16.9	511
15	10–3A	17.0	508
16	10–3B	16.9	511
17	10–4A	16.8	514
18	10–4B	17.0	508
19	10–5A	17.0	508
20	10–5B	17.0	508

1. Capacitance measured 17 June 77 by R. Popp.
2. $X_n = 8632.65/C$ where C is in picofarads and X_n is in angstroms.
3. Mean $\bar{X}_n = 511.05$ Å, standard deviation $S_{X_n} = 4.9$ Å, maximum $X_n = 523$ Å, minimum $X_n = 505$ Å, range $A_{X_n} = 18$ Å.

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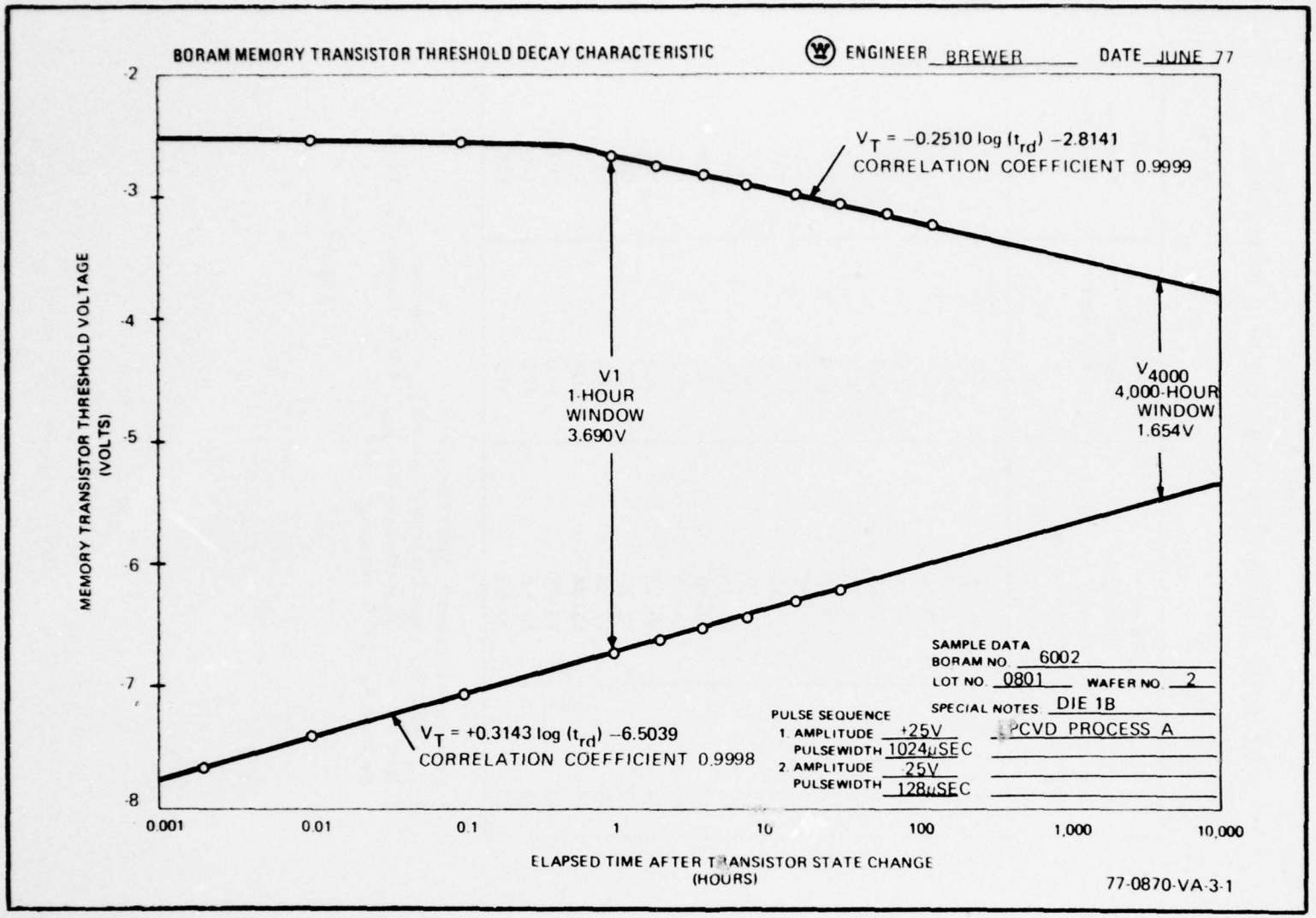

Figure 1-2. Typical Initial Threshold Decay Characteristic

The written state was established by applying a VGS pulse sequence of +25 volts for 3.6 seconds and -25 volts for 128 microseconds, repeated 16 times. Therefore, the transistor should be in a saturated clear state prior to the write pulse. The write is generally not sufficient to establish a saturated low conduction threshold.

Observations of the threshold voltage began at 0.001 hours (3.6 seconds) after termination of the write pulse. Additional measurements were taken at 0.01, 0.1, 1, 2, 4, 8, 16, 32, 64, and 128 hours. For individual parts, the observation sequence may have been terminated earlier than 128 hours.

In the set of 20 devices one transistor (reference number 10) was found to be nonfunctional. Another device (reference number 5) exhibited a very slow write decay rate. The remaining 18 parts had reasonably homogenous write decay slopes. The situation shown in figure 1-2 is typical. The decay can be fitted with high precision (correlation coefficient > 0.999) to the form:

$$V_T = r_{VW} \log t_{rd} + V_{1W}$$

r_{VW} write threshold decay slope (volts/decade)

t_{rd} read delay time (hours)

V_{1W} threshold voltage at 1 hour (volts)

V_T threshold voltage (volts)

The decay characteristic from the cleared state is slightly more complicated. The cleared state was established by a VGS pulse sequence of -25 volts for 3.6 seconds and +25 volts for 1024 microseconds, repeated 16 times. Therefore, the transistor should be in a saturated write state prior to application of the final clear pulse. As it will be shown later, the 1024 microsecond clear pulse is just adequate to push the threshold into the beginning of the saturated region for these particular samples.

After termination of the final clear pulse, the threshold voltage was observed at 0.001, 0.01, 0.1, 1, 2, 4, 8, 16, 32, 64 and 128 hours. For some samples the observation period was less than 128 hours.

The reason for inquiring into the decay characteristic of the memory transistor is to gain some insight as to how a memory cell will perform. In a simplified fashion, it can be said that a two-transistor cell detects data by comparing the thresholds of a transistor which has been cleared to the threshold of a transistor that has been written. Because the transistors are physically similar and are adjacent to each other in a memory array, the threshold difference can be estimated by examining the decay characteristics of a single transistor.

To facilitate analysis, it is helpful to define a quantity called the threshold window. The window is the algebraic difference between the clear decay curve and the write decay curve. It is a positive quantity until a one and zero can no longer be distinguished.

$$V_W = V_T \text{ (cleared)} - V_T \text{ (written)}$$

In the case of the LPCVD samples, both the cleared and written states for times greater than about 1 hour decay linearly with the logarithm of time. Therefore, the window decay can be expressed as:

$$V_W = r_V \log t_{rd} + V_1$$

r_V window decay rate (volts/decade)

t_{rd} read delay time (hours)

V_1 window voltage at 1 hour (volts)

V_W window voltage (volts)

The clear decay characteristic shown in figure 1-2 was typical. From 0.001 hours until 1 or 2 hours the observed decay rate was quite low. It is assumed that during this interval the nonmemory portion of the drain-source protected (DSP) memory transistor is dominating the threshold characteristic. After the 1- or 2-hour measurement a greater decay rate is observed. It appears that the threshold of the memory portion of the DSP transistor has become dominant, and can be observed directly. Like the write decay

characteristic, the last portion of the clear decay characteristic can be fitted with high precision (correlation coefficient >0.999) to the form:

$$V_T = r_{VC} \log t_{rd} + V_{1C}$$

r_{VC} cleared threshold decay slope (volts/decade)

t_{rd} read delay time (hours)

V_{1C} threshold voltage at 1 hour (volts)

V_T threshold voltage (volts)

From the previous development of the clear and write decay equations, it can be seen that:

$$r_V = r_{VC} - r_{VW}$$

$$V_1 = V_{1C} - V_{1W}$$

For a viable memory cell r_V is a negative quantity, and V_1 is a positive quantity. The window can be plotted as a decreasing straight line in the first quadrant against log time, or window values can simply be noted on the composite clear and write decay curves. On figure 1-2, the V_1 value has been labeled.

Because the BORAM retention goal is 4,000 hours, it is of interest to note the window at that time. V_{4000} is also labeled in figure 1-2.

If an ideal detector were available (i.e., capable of detecting any difference greater than zero), the time at which the window closed to zero volts would represent the retention period. This time t (0V) is used by some workers in the MNOS field as a retention figure of merit. A companion parameter is the device threshold voltage value at which the window converges to zero V (0V).

The detection circuit used in the BORAM 6002 chip can distinguish 0.1 volt differences. Therefore, the time t (0.1V) at which the window closes to 0.1 volts is a maximum possible retention expectation.

In practice the two transistors in a memory cell cannot be identical. Therefore, some margin must be allowed over the detection capability of the sense circuit. Arbitrarily t (0.3V) has been chosen to approximate a practical retention time projection.

These numbers should be interpreted as comparative figures of merit - not as actual statements of in system data retention time. The values are very sensitive to pulse amplitude and duration, and are prone to be very adverse because of testing guard bands with respect to actual use conditions. The important aspect of their application is that a standard set of test conditions be employed so that sample comparisons can be meaningful.

Table 1-2 provides a tabulation of these parameters for the set of 20 samples. Table 1-3 shows the mean an standard deviation for each parameter. The uniformity of the characteristics was quite remarkable.

1.1.3 Pulse Response Characteristics

The pulse response from a saturated state was also explored for the 20 samples from lot 0801. Figure 1-3 shows the write and clear response characteristic curves for six different pulse amplitudes overlayed on one graph. The form of these curves was typical of the population.

The so called pulse response curve is a plot of threshold voltage against the pulsewidth of the applied gate voltage. Normally, the pulsewidth scale is logarithmic. This means of displaying the dependance of threshold shift on pulse duration has come to be common practice. Quantitative values for a given curve depend on ground rules for the measurements, and these details must always be clearly stated.

One point on a write pulse response curve is obtained by initially shifting the threshold to a saturated clear level, pulsing the gate with a fixed amplitude and duration write pulse, and then measuring the threshold after a specified time delay. The procedure is repeated with a new pulsewidth to obtain additional data points. A clear response curve is similar, except that the clearing and writing pulses are interchanged.

TABLE 1-2

LOT 0801 SAMPLES INITIAL THRESHOLD DECAY OBSERVATIONS

Reference Number	Clear Decay Rate r_{VC} V/decade	Write Decay Rate r_{VW} V/decade	Window Decay Rate r_V V/decade	Window at 1-hour V_1 volts	Window at 4,000 hours V_{4000} volts	Time to 0.3 volt Window t (0.3V) hours	Time to 0.1 volt Window t (0.1V) hours	Time to 0 volt Window t(0V) hours	Convergence Voltage for 0V Window V(0V) volts
1	0.2510	0.3143	0.565	3.690	1.654	9.9E5	2.2E6	3.4E6	4.45
2	0.2724	0.3403	0.613	4.065	1.857	1.4E6	3.0E6	4.3E6	4.47
3	0.2741	0.2692	0.543	3.730	1.773	2.1E6	4.8E6	7.3E6	4.56
4	0.1951	0.3387	0.543	3.943	2.020	6.7E5	1.6E7	2.4E7	4.19
5	0.2634	0.0566	0.320	1.881	0.728	8.7E4	3.7E5	7.5E5	4.25
6	0.2677	0.3188	0.587	4.023	1.911	2.2E6	4.9E6	7.2E6	4.46
7	0.2486	0.3046	0.553	3.647	1.655	1.1E6	2.6E6	3.9E6	4.76
8	0.2401	0.3341	0.574	3.915	1.847	2.0E6	4.4E6	6.6E6	4.68
9	0.2183	0.3317	0.550	3.818	1.837	2.5E6	5.7E6	8.7E6	4.50
10	———	———	Sample does not function as a memory transistor				———	———	———
11	0.2118	0.2827	0.495	3.505	1.724	3.0E6	7.7E6	1.2E7	4.70
12	0.2425	0.3080	0.551	3.650	1.667	1.2E6	2.8E6	4.3E6	4.53
13	0.2041	0.3462	0.550	3.980	1.925	3.6E6	8.3E6	1.3E7	4.38
14	0.2043	0.2184	0.423	3.172	1.649	6.2E6	1.8E7	3.2E7	4.51
15	0.2094	0.3301	0.540	3.746	1.802	2.4E6	5.7E6	8.8E6	4.50
16	0.2226	0.2909	0.514	3.573	1.724	2.4E6	5.8E6	9.1E6	4.49
17	0.2124	0.3006	0.513	3.620	1.772	3.0E6	7.3E6	1.1E7	4.85
18	0.1943	0.3247	0.519	3.739	1.870	3.2E6	1.0E7	1.6E7	4.44
19	0.1744	0.2484	0.423	3.387	1.864	2.0E7	6.0E7	1.0E8	4.27
20	0.2242	0.2462	0.470	3.388	1.693	3.7E6	9.7E6	1.6E7	4.43

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TABLE 1-3

LOT 0801 SAMPLES INITIAL THRESHOLD DECAY STATISTICS

Parameter	Symbol	Units	Mean $\bar{X}$	Standard Deviation σ
Clear decay rate	r_{VC}	V/decade	−0.2279	0.0293
Write decay rate	r_{VW}	V/decade	0.2897	0.0668
Window decay rate	r_V	V/decade	−0.518	0.069
Window at 1 hour	V_1	volts	3.604	0.478
Window at 4000 hours	V_{4000}	volts	1.735	0.266
Time to 0.3 volts window	t (0.3V)	hours	2.1E6[1]	2.91[2]
Time to 0.1 volts window	t (0.1V)	hours	2.7E6[1]	2.78[2]
Time to 0 volts window	t (0V)	hours	9.0E6[1]	2.75[2]
Convergence voltage for 0 volts window	V (0V)	volts	−4.50	0.17

1. Mean value of the logarithm of the time values.
2. Coefficient of variation $\sigma/\bar{X}$ which is a numeric.

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The Westinghouse VT tester gathers this automatically and stores in a memory for recall. The read delay time is 3.6 seconds. Pulsewidths follow the sequence 1, 2, 4...512, 1024 microseconds. Thresholds are measured at a drain current of 10 microamperes.

Pulse response is very important to proper operation of memory transistors in an integrated circuit array. In fact, the previously presented decay characteristic data actually contains a great amount of information related to pulse response. There the question was, does the memory transistor exhibit a combination of pulse response (window) and decay slope compatible with retention objectives.

For the pulse response characteristic curves more subtile considerations are involved. It is possible to use this data (in combination with some additional measurements) to quantify many of the parameters in device switching models.

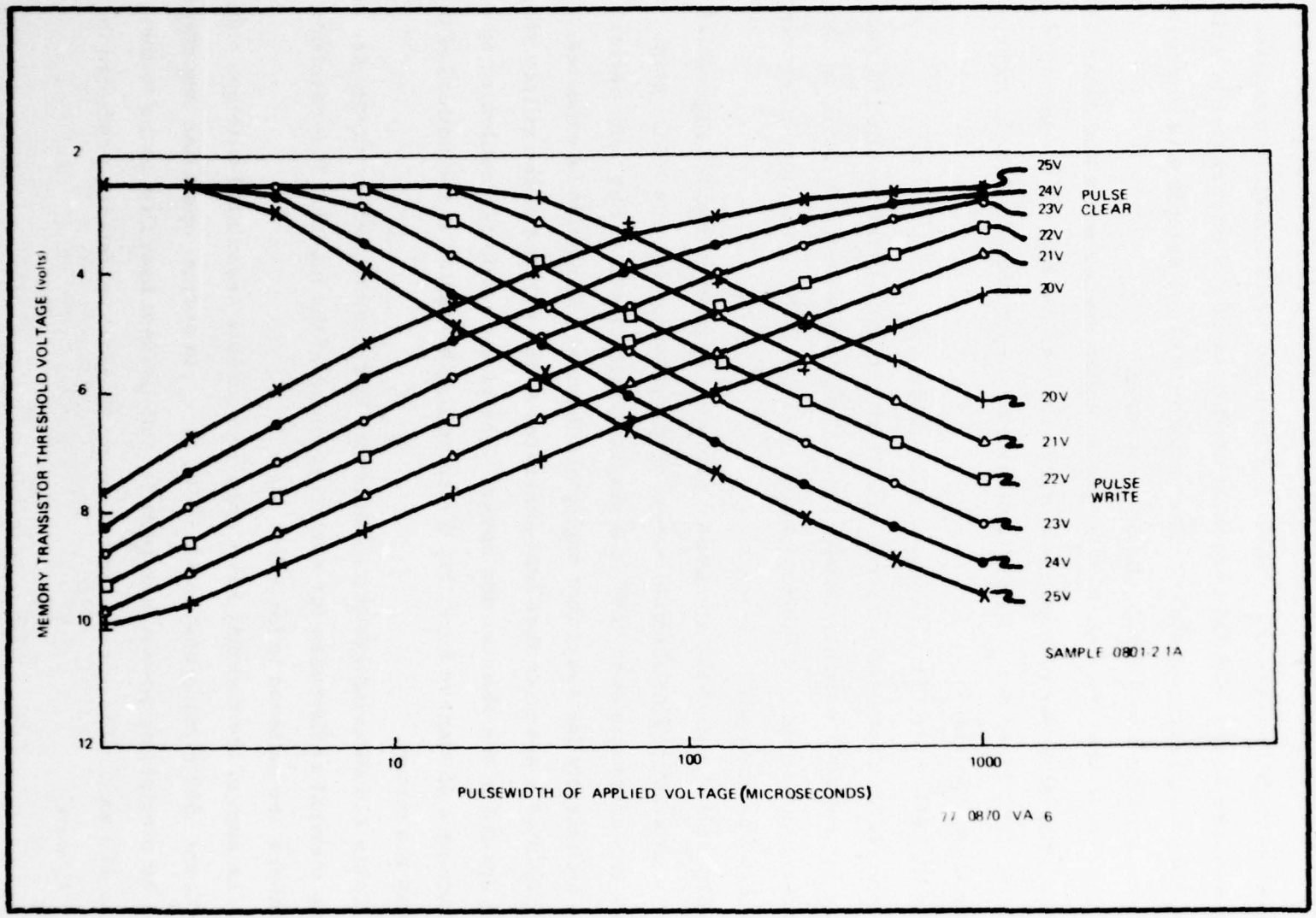

Figure 1-3. Typical Pulse Response Characteristic

For the sample of 20 devices only a few of the more salient points of interest have been examined. Table 1-4 lists the write and clear response of the samples at the BORAM screening conditions of 128 microseconds write and 1024 microseconds clear. The uniformity of the sample was impressive. Device number 5 was really the only maveric.

This table also lists the beta tunneling constants for write and clear. The write beta value was obtained by a curve fit over the 8 to 64 microsecond data points. The clear beta value was obtained by a fit over the 2 to 16 microsecond data points.

1.2 HYBRID CIRCUIT THERMAL ANALYSIS

Knowledge of the temperature rise from the case to the junction is necessary for reliability model calculations. To provide an upper bound on thermal resistance a simplified thermal analysis of the BORAM memory microcircuit has been performed.

Figure 1-4 shows the component parts of the microcircuit. Figure 1-5 provides a simplified thermal model of the situation for one MNOS chip. Only two chips are ever "on" in a single hybrid circuit. The "on" devices are sufficiently far apart that negligible thermal interaction is expected.

The model assumes that heat generated at the surface of the silicon chip will spread in the alumina and kovar. The cross section is estimated by assuming a 45-degree angle for the spreading beginning at the bottom of the epoxy die mount.

Table 1-5 summarizes the conductivity and dimensional assumptions, and lists thermal resistances for each component of the model. The resulting numbers are believed to be worst case.

The sum of the thermal resistance components associated with one chip (BORAM 6002 dimensions) is 10.59°C/watt. In normal operation two chips will be dissipating power, and parallel independent heat flow paths to the case will exit. Therefore, the maximum thermal resistance predicted is 5.3°C/watt.

TABLE 1-4

SOME PULSE RESPONSE PARAMETERS FOR LOT 0801 SAMPLES

Device Reference Number	Write Response $t_w = 128\mu sec$ V_T volts	Clear Response $t_w = 1024\mu sec$ V_T volts	Write $\partial V_T/\partial \ln t_w$ β^- (volts/decade)/ln 10	Clear $\partial V_T/\partial \ln t_w$ β^+ (volts/decade)/ln 10
1	7.395	2.610	1.27	−1.07
2	7.695	2.585	1.21	−1.07
3	7.170	2.565	1.32	−1.17
4	7.660	2.680	1.22	−1.14
5	4.650	2.615	0.53	−0.53
6	7.540	2.610	1.26	−1.13
7	7.630	2.910	1.26	−1.08
8	7.905	3.010	1.23	−1.08
9	7.730	2.700	1.21	−1.03
10[1]	–	–	–	–
11	7.485	2.815	1.30	−1.07
12	7.460	2.685	1.27	−1.08
13	7.790	2.675	1.20	−1.15
14	6.815	2.860	1.37	−1.19
15	7.715	2.735	1.22	−1.12
16	7.380	2.720	1.28	−1.13
17	7.815	3.090	1.27	−1.10
18	7.905	3.080	1.22	−1.08
19	6.950	2.720	1.40	−1.09
20	6.935	2.740	1.40	−1.09
Mean[2]	7.499	2.766	1.27	−1.10
Standard[2] Deviation	0.336	0.163	0.06	0.04

1. Part 10 was nonfunctional
2. Part 5 and 10 were excluded from the population.

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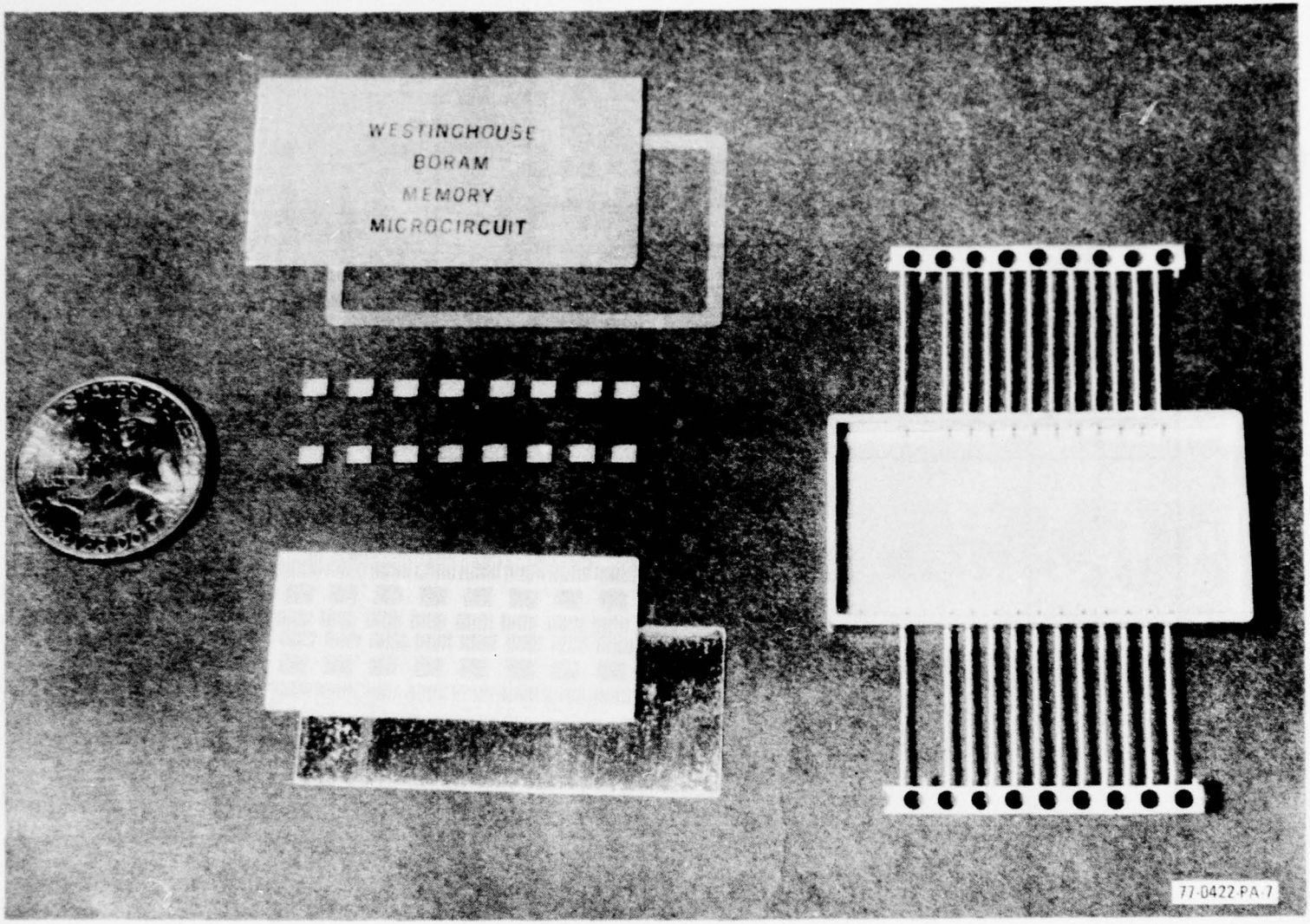

Figure 1-4. Component Parts of BORAM Memory Microcircuit
Westinghouse Part 647R527G01

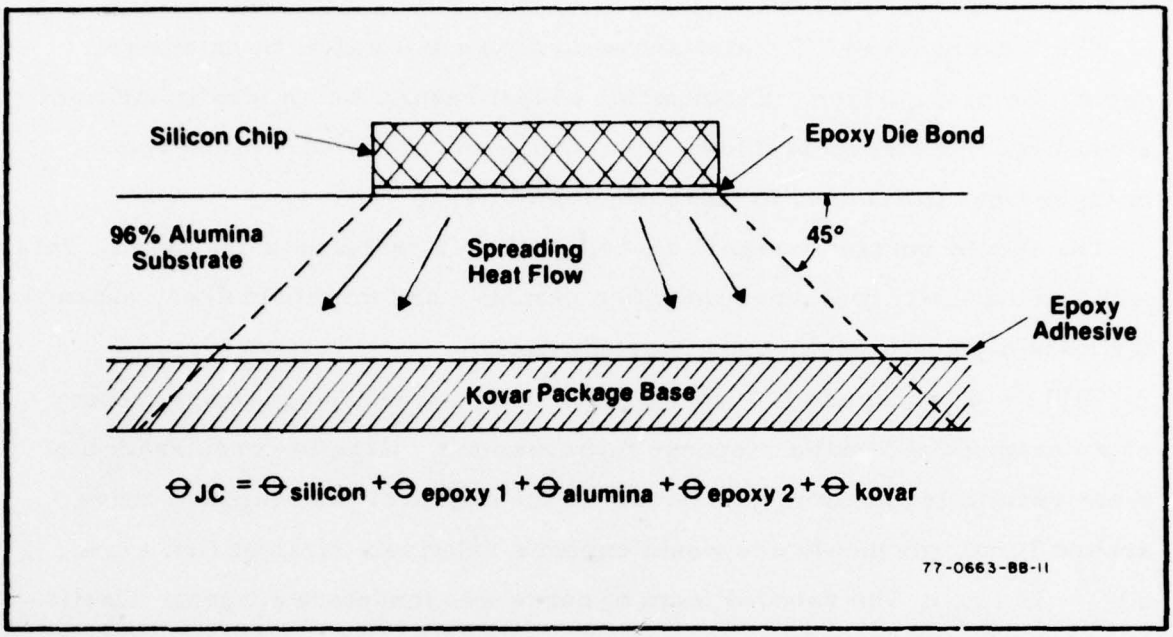

Figure 1-5. MNOS BORAM Hybrid Circuit Simplified Thermal Model

TABLE 1-5

MNOS BORAM HYBRID CIRCUIT THERMAL RESISTANCE COMPONENTS

Material	Thermal Conductivity K watts/inch ^{o}C	Material Thickness t inches	Effective Cross-Section (ℓ) (ω) inches^2	Thermal Resistance θ ^{o}C/watt
Silicon	3.60	0.016	(0.099) (0.128)	0.35
Epoxy	0.025	0.001	(0.099) (0.128)	3.16
Alumina	0.670	0.046	(0.145) (0.174)	2.72
Epoxy	0.020	0.003	(0.194) (0.223)	3.47
Kovar	0.420	0.020	(0.217) (0.246)	0.89

$\theta = t/K\ \ell\ \omega$

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1.3 VT TESTER STATUS

The Westinghouse VT tester shown in figure 1-6 was used extensively during the past quarter. Examination of test results led to identification of some lingering circuit problems that have been corrected. Also, some changes were introduced to increase flexibility.

The second quarterly report described the VT tester in some detail. This unit automatically measures the pulse response and threshold decay characteristics of one- to eight-transistor samples.

Table 1-6 and figure 1-7 were presented in the second quarterly report as an example of a pulse response measurement. Careful consideration of these results led to some questions. In the region of the response curve around 10 microseconds one would expect a relatively straight line - i.e., $\Delta V_T \approx \ln t_{PW}$. The rounded form of curve was therefore suspect. Oscilloscope observation of the write pulses revealed that the proper pulsewidths were not maintained for the short time values.

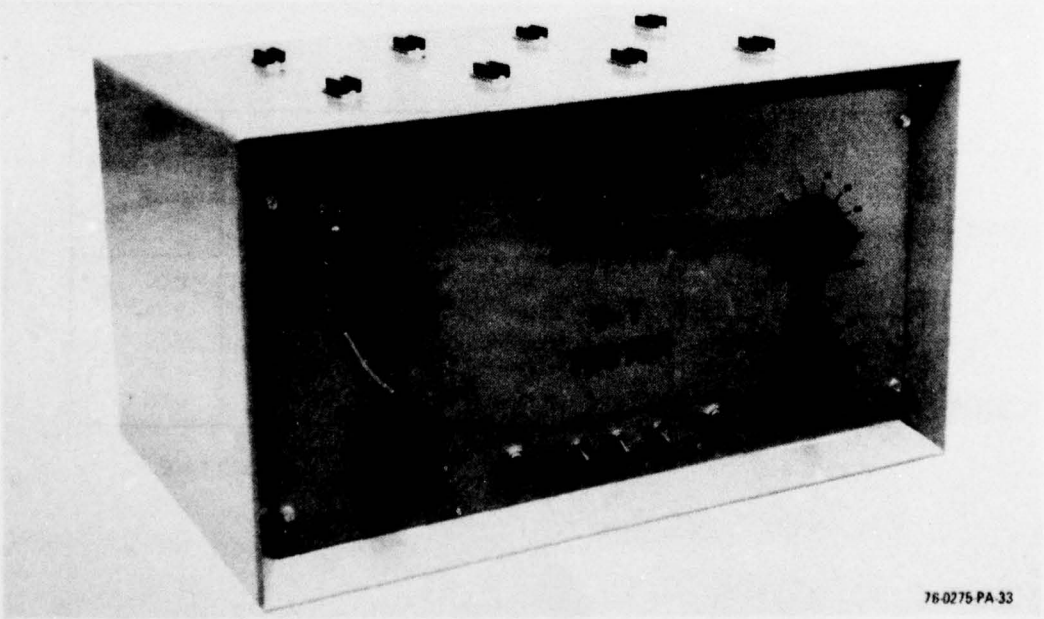

Figure 1-6. The Westinghouse VT Tester

TABLE 1-6

EARLY WRITE PULSE RESPONSE MEASUREMENTS

Write Pulse-width μsec	Threshold Voltage VT at 10 μA (Volts)		
	Sample 2838A-1	Sample 2838A-2	Sample 2838A-3
1	2.995	2.830	2.820
2	3.075	4.185	2.855
4	4.115	6.830	5.095
8	5.060	8.125	6.205
16	5.695	8.885	6.755
32	6.205	9.415	7.100
64	6.595	9.785	7.335
128	6.850	10.015	7.485
256	6.975	10.130	7.525
512	6.995	10.155	7.495
1024	6.990	10.155	7.465

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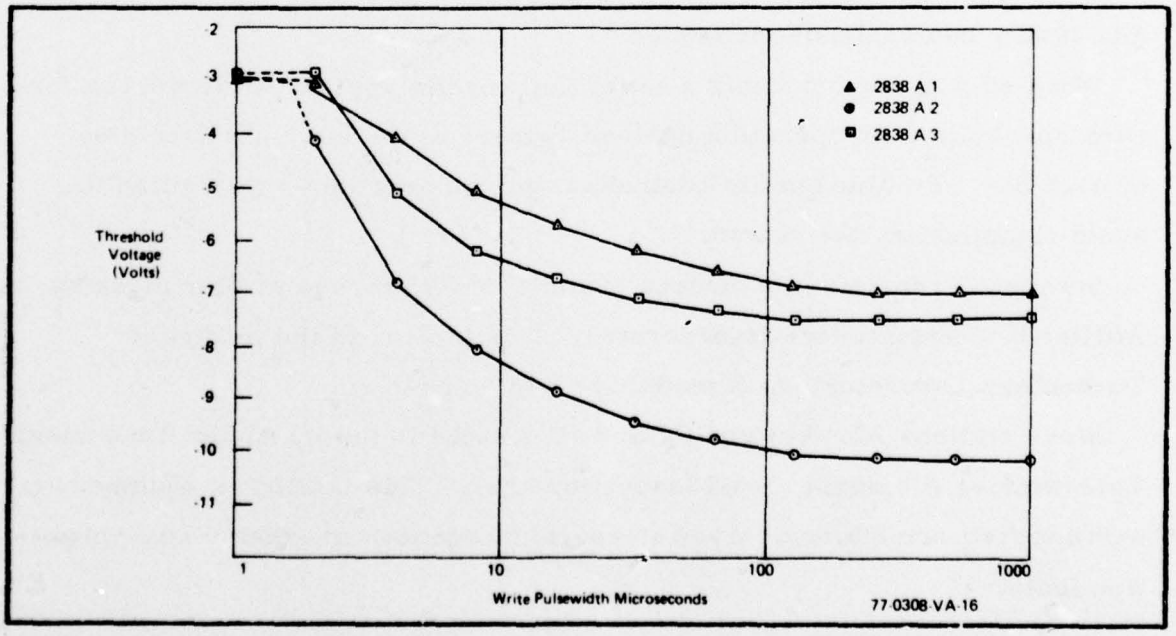

Figure 1-7. Early Write Pulse Response Measurements

After circuit corrections were made, the pulse response observations assumed the expected form. Figure 1-3 under paragraph 1.1 is an example of a typical characteristic.

After using the VT tester for some time, it was found to be desirable to be able to vary the pulse amplitudes for different experiments. The internal supplies were disconnected, and a cable was brought out to external laboratory supplies. A digital bridge type voltmeter was connected to the supplies through a special switch arrangement to allow the rapid setting of accurate voltage levels.

Because of this modification, the tables in the second quarterly report presenting the test sequence details need to be updated to show variable voltage levels. Table 1-7 and 1-8 are the revised tables.

1.4 PRODUCTION LINE DEFINITION

The processing sequence used to produce the MNOS BORAM hybrid circuits is defined in figures 1-8 and 1-9. Figure 1-8 treats the processes which are performed on every hybrid package. Figure 1-9 shows the routing required for samples taken from the production line for confirmatory sample and quality conformance inspection.

Work station numbers with a letter code prefix appear inside the box for each operation. An operation number appears at the top right hand side of each box. Routine quality control sampling operations are omitted to avoid complicating the charts.

Station A1 consists of a Presco Model 645 silk-screen printer made by Affiliated Manufacturers Incorporated. It is located in the Advanced Technology Laboratories, E module hybrid laboratory.

Work stations A2, A13 and C7 are all located in the Advanced Technology Laboratories A module visual inspection area. This facility is equipped with a variety of metalurgical and stereo microscopes and other visual inspection tools.

TABLE 1-7

VT TESTER THRESHOLD DECAY TEST SEQUENCES

TYPE TEST	TEST PROGRAM SEGMENT	ELECTRICAL TEST CONDITIONS
CLEAR THRESHOLD DECAY	Precondition Sequence (repeated 4 times)	1. Write VGS = −XV, 3.6 sec 2. Clear VGS = +YV, 1024 μsec
	Decay Time Test Sequence (maximum read delay time is selected by the DECAY TIME DURATION switch)	Read VHC threshold at 10 μA for read delay times of 0.001 hr, 0.01 hr, 0.1 hr, 1 hr, 2 hr, 4 hr, 8 hr, 16 hr, 32 hr, 64 hr, and 128 hr.
WRITE THRESHOLD DECAY	Precondition Sequence (repeated 4 times)	1. Clear VGS = +YV, 3.6 sec 2. Write VGS = −XV, 128 μsec
	Decay Time Test Sequence (maximum read delay time is selected by the DECAY TIME DURATION switch)	Read VHC threshold at 10 μA for read delay times of 0.001 hr, 0.01 hr, 0.1 hr, 1 hr, 2 hr, 4 hr, 8 hr, 16 hr, 32 hr, 64 hr, and 128 hr.

Note: X and Y voltages are adjustable externally

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TABLE 1-8

VT TESTER PULSE RESPONSE TEST SEQUENCES

TYPE TEST	TEST PROGRAM SEGMENT	ELECTRICAL TEST CONDITIONS
CLEAR PULSE RESPONSE	Precondition Sequence (repeated 3 times)	1. Write VGS = −XV, 3.6 sec 2. Clear VGS = +YV, 1024 μsec
	Response Test Sequence Auto Mode: Scanned for 11 values of n (1, 2, 4, 8 ... 512, 1024). Manual Mode: Only 1 value of n selected by MANUAL PULSEWIDTH switch.	1. Write VGS = −XV, 3.6 sec 2. Clear VGS = +YV, n μsec 3. Delay 3.6 sec 4. Read VHC threshold at 10 μA
WRITE PULSE RESPONSE	Precondition Sequence (repeated 3 times)	1. Clear VGS = +YV, 3.6 sec 2. Write VGS = −XV, 128 μsec
	Response Test Sequence Auto Mode: Scanned for 11 values of n (1, 2, 4, 8 ... 512, 1024). Manual Mode: Only 1 value of n selected by MANUAL PULSEWIDTH switch.	1. Clear VGS = +YV, 3.6 sec 2. Write VGS = −XV, n μsec 3. Delay 3.6 sec 4. Read VLC threshold at 10 μA

Note: X and Y voltages are adjustable externally

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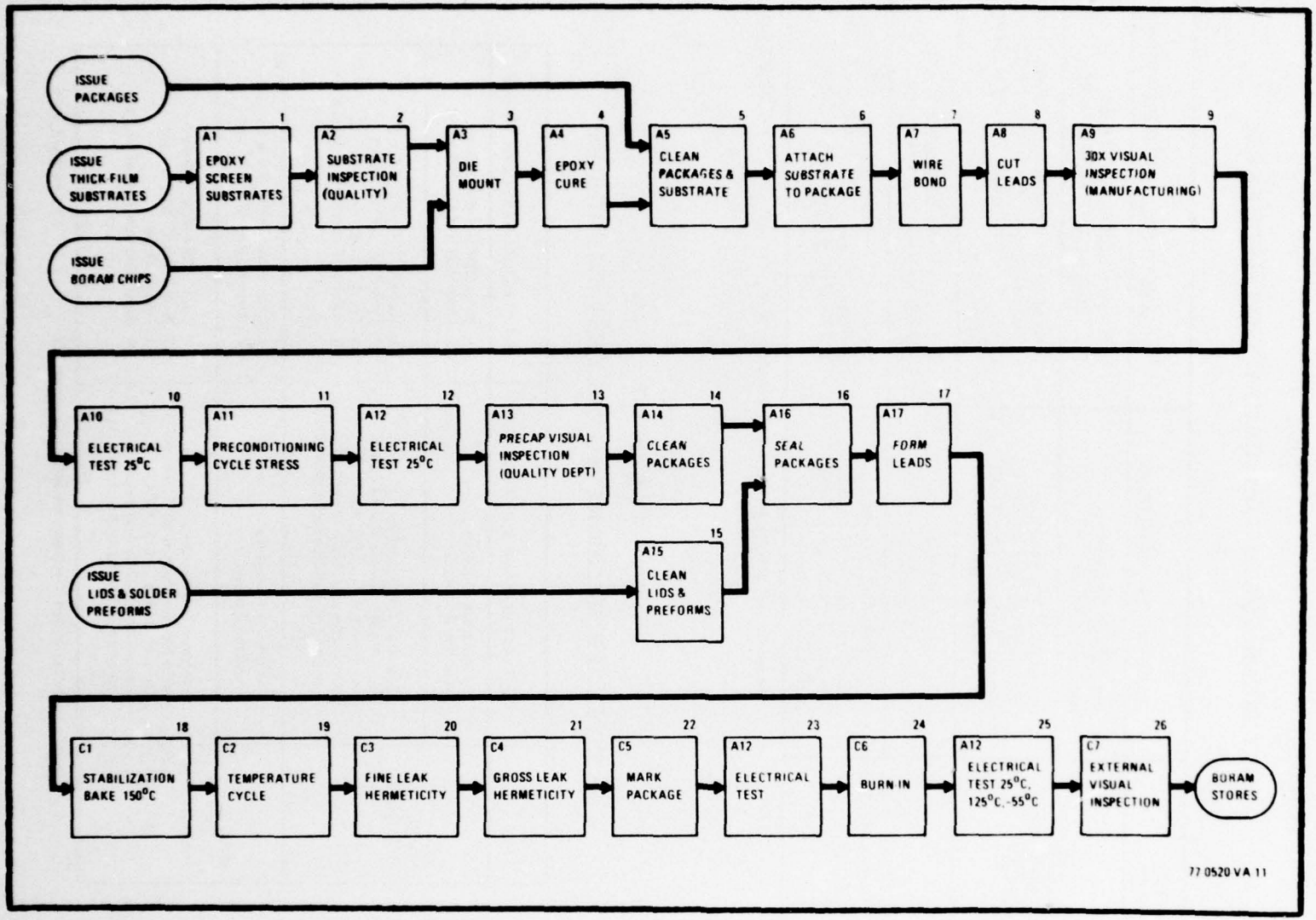

Figure 1-8. MNOS BORAM Hybrid Production Processing Sequence

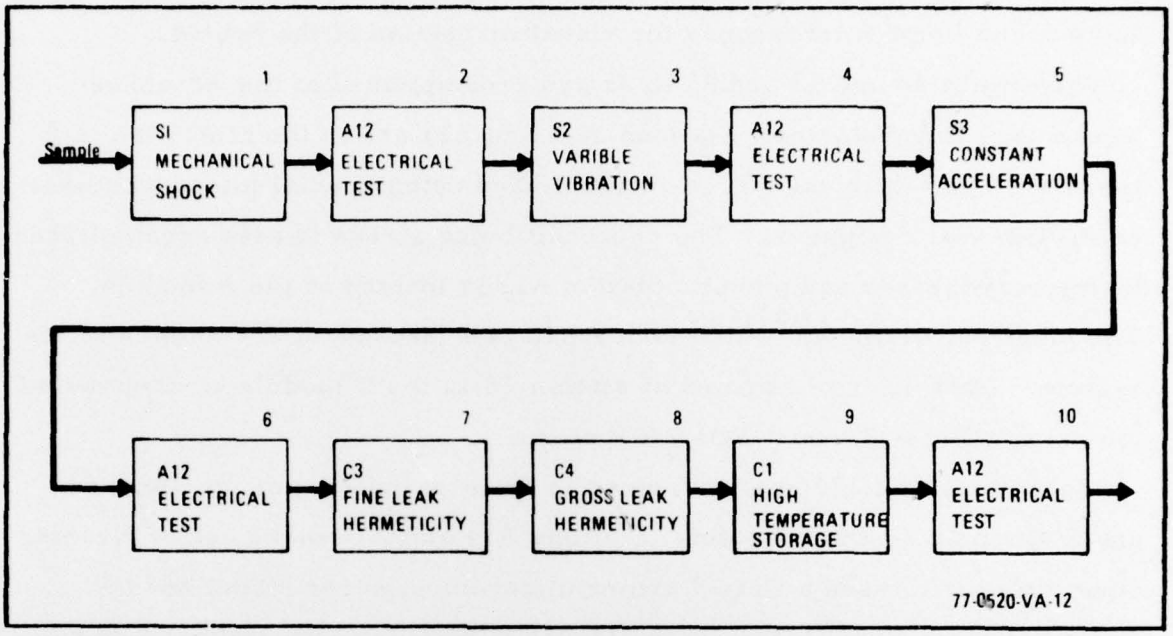

Figure I-9. Sample Tests Required by SCS-503 for Confirmatory Sample and for Quality Conformance Inspection

Stations A3 to A9 are located in the east building of the Defense and Electronic Systems Center. The central items of equipment employed at each station are as follows. A3 makes use of a Model E-752 die bonder made by Mech-el Industries. Station A4 uses a Blue-M Electric Company Power-O-Matic 60 B-3005-6 chamber. A variety of apparatus is employed at station A5 for cleaning packages, substrates and preforms. This includes a Model 8845-6 ultrasonic cleaner made by Cole-Parmer Instrument Company, a Hotpack vacuum oven, cleaning chemicals, nitrogen blowoff lines, and glassware. Station A6 accomplishes substrate to package attachment in a system made by CHA Industries. Station A7 uses a computer controlled wire bonder. The controller was manufacturered by Gaiser Tool Company to Westinghouse specifications. Bonding programs are stored on a floppy disc. The controlled bonder is a K&S Model 478. Package leads are cut to size at station A8 using equipment made by Owatonna Tool

Company. Station A9, is equipped with several American Optical and Bausch and Lomb microscopes for visual inspection of the hybrid.

Operations 10 and 13 and 23 to 26 are accomplished at the Advanced Technology Laboratories. Stations A10 and A11 are in the MNOS lab in D module. The electrical test is accomplished using special microprocessor controlled test equipment. The preconditioning stress is also accomplished by microprocessor equipment. Station A12 is located in the A module. The principal equipment which forms A12 is a Macrodata 154 automatic test system. Burn-in is performed at station C6 in the C module environmental lab using a Blue-M model FOM246E oven.

Operations 14 to 22 are performed in the east building of the Defense and Electronic Systems Center. Stations A14 and A15 make use of cleaning chemicals. A15 uses a Cole-Parmer ultrasonic cleaner Model 8845-6. Packages are sealed at A16 using Model 6FP4 automatic sealer made by Research Instrument Company. Leads are formed at A17 by a press made by Owatonna Tool Company. At C1, the stabilization bake is performed in a Hotpack Model 1258-3 oven. A Standard Environmental System Incorporated Model LHTS/15H chamber is used at station C2 for temperature cycling. At C3, fine leaks are detected using a Norton mass spectrometer Model 925. Gross leak check at station C4 uses a Trio-Tech Incorporated Model A-481. Packages are marked at C5 using a Markem Model 1300.

The sample operations shown in figure 1-8 use some of the equipment previously described. Stations S1, S2 and S3 are located in the Product Qualification Laboratory. This facility performs environmental, qualification, reliability, sampling and development tests for all divisions of the Defense and Electronic Systems Center, and is fully instrumented for mechanical shock, variable vibration, and constant acceleration testing.

1.5 PRODUCTION ACTIVITY

During the fourth quarter of effort, all of the chips necessary to provide the second set of engineering samples and the confirmatory samples were

produced. Initial yield experience was gained with the 6002 device. Experiments with computer controlled wire bonding of the hybrid were encouraging.

1.5.1 BORAM 6002 Production

BORAM 6002 dice for engineering samples and confirmatory samples were produced on two-inch wafers. Table 1-9 summarizes the wafer and die production. Table 1-10 presents the yield experience. These die were tested using a 200 microsecond clear and 100 microsecond write criteria, and a 2.5 msec clear and 1 msec write. The bulk of the population was found to qualify to a 1 msec clear and 200 microsecond write criteria. Sawing and visual yields are omitted because many of the parts are being retained in wafer form until hybrid assembly is ready to begin.

As a first effort the production results were encouraging. Previous efforts with the 6000C chip resulted in 1090 functional die from 727 wafers, or about 1.5 die per wafer start. For the initial 6002 chips 1178 die were obtained from 110 wafers, or about 11 die per wafer start.

TABLE 1-9

INITIAL BORAM 6002 PRODUCTION SUMMARY

Item Produced	Quantity
Wafers Started	110
Wafers Completed	69
Chips Completed	1178

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TABLE 1-10

INITIAL BORAM 6002 YIELD EXPERIENCE

Yield Component	Symbol	Target Yield	Actual Yield
Process Yield	Y_W	0.70	0.63
Probe Yield	Y_T	0.10	0.09
Overall Yield	Y	0.07	0.06

77-0870-TA-10

The 6002 yield was depressed by a problem with P+ diffusion uniformity and by some contact problems. Probe test experience reflected these difficulties, and yields per wafer were broadly scattered. As happened with the 6000C, the 6002 yield is expected to rise sharply after an initial learning period.

In expectation of start-up difficulties a modest goal of 0.10 was set for the 6002 probe yield. Mathematical models predict that an average yield of 0.38 is obtainable. Actual experience showed 26 wafers that exceeded the 0.10 goal. The highest yield was 62 die on a single two-inch wafer, or about 0.32.

1.5.2 Wirebonding Progress

Potentially the largest labor content item associated with the production of the hybrid circuit is wire bonding. With 16 chips in a package about 528 bonds (264 wires) must be made. To reduce the labor cost, to improve reliability, and to increase production throughput computer controlled bonding of the BORAM hybrid is being developed.

The Westinghouse automatic wirebonder consists of an ultrasonic bonder, master console, a disk memory, an operators control pendant and a power

supply. Programming and bonding is accomplished from the master control console. A microprocessor directs the automatic operations. The bonding program is stored on the disk memory.

Initial bonding experiments with BORAM substrates have been successful. Automatic bonding of the 16 chips has been achieved. Hundreds of test bonds have been made and destructively pulled. The results indicate good bond integrity. The primary failure mode was wire breaks.

It appears that the use of computer controlled bonding will offer significant throughput advantages over manual bonding. Initial data indicates that a single automatic station can bond at least six times faster than a manual station. In addition, one operator can easily control two automatic stations.

2. CONCLUSIONS

The introduction of LPCVD nitride has greatly improved the uniformity of device characteristics. Embryo production experience with the new 6002 chip has already surpassed yield levels achieved with the more mature 6000C. Chip production requirements for engineering and confirmatory samples have been met. The hybrid circuit production line has been completely defined, and detailed implementation is underway.

The major problem area for the project continues to center around test development, and the time required for proper evaluation of product and process alternatives. During the next two quarters these issues will be the primary focus of the engineering effort.

3. PROGRAM FOR NEXT INTERVAL

The primary task during the next quarter is the detailed design of the test stations required for hybrid circuit production. Evaluation of process results using transistor structures will be another priority task. The assembly of the engineering sample hybrids will also be accomplished.

4. PUBLICATIONS AND REPORTS

During the past quarter there were no publications derived directly from this contract effort.

5. IDENTIFICATION OF TECHNICIANS

The following key engineers and management personnel were employed on the BORAM manufacturing methods project during April, May and June of 1977.

Technician	Manhours
J. Brewer	376
R. Popp	312
M. Peckerar	12
C. Walvogel	64
T. O'Donnell	36
P. Smith	178
L. Epstein	53

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